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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/609,264	06/26/2003	Nicholas G. Samra	42P16354	8108

7590 01/05/2006

EXAMINER	
CODY, DILLON J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 01/05/2006

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/609,264	SAMRA ET AL.	
	Examiner	Art Unit	
	Dillon Cody	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 June 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12 Oct. 2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-30 are pending.

Papers Filed

2. Examiner acknowledges receipt of drawings, claims and specification, filed 26 June 2003; declaration filed 14 October 2003; and information disclosure statement filed 12 October 2005.

Title

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Drawings

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: local bus 307.

5. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "330" in Figure 3 has been used to designate both Network Interface and Wireless Interface.

6. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following not mentioned in the description: Wireless Interface.

7. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

8. The disclosure is objected to because of the following informalities:

-Paragraph 16, line 1: "operation" should read "operations".

-Paragraph 24, line 2: ""in" should follow "increase".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

9. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 14-15 and 29-30 rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which

was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The disclosure teaches reserving a block of registers for a second thread while the processor is running in Single Threaded mode in paragraphs 24-25 and Fig. 5. With these physical registers reserved for the second thread, the sum of free registers and those used by the first thread cannot equal the total number of physical registers, as required by claims 14 and 29. The claim language requires that when in ST mode, all of physical registers that are unused by the first thread must be in the free list.

10. Claims 15 and 30 are rejected based on their dependencies.

Claim Rejections - 35 USC § 101

11. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

12. Claims 14 and 29 are rejected under 35 U.S.C. 101 because the claimed invention lacks patentable utility. If the processor is running in Multithreaded (MT) mode, the claim language requires that no registers be associated with the second thread. Since the total number of physical registers equals the number of those in the free list plus the number of registers associated with the first thread, no physical registers can be associated with the second thread. If the second thread cannot have any registers in which to store data, the thread cannot be processed on the processor.

Claim Rejections - 35 USC § 102

13. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

14. Claims 1-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Levy et al. (U.S. Patent No. 6,092,175) hereinafter referred to as Levy.

15. As per claim 1, Levy discloses an apparatus comprising: a physical register file (Fig. 1 register file 37) in which data associated with instructions of a computer program are stored in an order that is independent of whether a processor executing the instructions is in a multithread (MT) mode or a single-thread (ST) mode. *The examiner asserts that the order in which data is stored in the register file is not dependant of how many threads are running, but rather which registers are available to the running threads. Fig. 15*

16. As per claim 2, Levy discloses the apparatus of claim 1 further comprising at least one register allocation table (RAT) (Fig. 4 register mapping table 72) to indicate allocation of the data from logical registers to physical registers within the physical register file. (Col. 9 lines 27-32)

17. As per claim 3, Levy discloses the apparatus of claim 1 further comprising a list of physical registers (Fig. 4 free register list 70) within the physical register file that are

not allocated to a logical register, (Col. 9 line 31-32) entries in the list being completely allocated to a first thread while the processor is in ST mode and entries in the list being partitioned such that a first portion of the entries are allocated to a first thread and a second portion of the entries are allocated to a second thread while the processor is in MT mode. *Levy's 2nd embodiment (described in Col. 10 lines 5-17 and pictured in Fig. 5B) fulfills the requirements of this claim. When only one thread is running, that thread has access to all of the renaming registers common to any running threads. When two threads are running, they share the common renaming registers and a partition can be made between registers associated with the first and second threads.*

18. As per claim 4, Levy discloses the apparatus of claim 3 wherein a first portion (Fig. 5B registers 86 in combination with the renaming registers) of all of the physical registers in the physical register file are allocated to the first thread and a second portion (Fig. 5B registers 88) of all of the physical registers in the physical register file are allocated to the second thread if the processor is in ST mode, the first portion of all of the physical registers being larger than the second portion of all of the physical registers. *The examiner asserts that if the processor is in ST mode, only one thread is running. This thread, therefor, has exclusive access to the shared renaming registers. Since the 2nd embodiment discloses that each thread has reserved architectural registers, regardless of whether there is an active thread associated with said thread or not, each of the first and second thread has a portion of the physical register file reserved for it.*

19. As per claim 5, Levy discloses the apparatus of claim 4 wherein the second thread is dormant if the processor is in ST mode. *The examiner asserts that if the processor is in Single-thread mode, only one thread is running. Inherently, any second thread cannot be running, and must therefor be dormant.*

20. As per claim 6, Levy discloses the apparatus of claim 4 wherein the first portion of all of the physical registers within the physical register file remain allocated to the first thread after the processor transitions to MT mode until instructions associated with data within the first portion of all of the physical registers within the physical register file are retired. *The examiner asserts that the processor disclosed by Levy inherently does not reallocate a currently used physical register to a newly started thread until the instruction(s) associated with said register are retired. (Col. 16 lines 39-44)*

21. As per claim 7, Levy discloses the apparatus of claim 6 wherein the physical registers associated with the retired instructions are indicated within the list of physical registers. (Col. 16 lines 39-44) *The examiner asserts that since a register's "contents may be overwritten" the register is added to freelist 70.*

22. As per claim 8, Levy discloses an apparatus comprising: first means (Fig. 4 free list 70) for indicating registers within a physical register file for use by a microprocessor that are not allocated to logical registers, the first means being partitioned during a

second mode of operation of the microprocessor and not being partitioned during a first mode of operation of the microprocessor; second means (Fig. 4 register mapping table 72) for allocating the logical registers to the physical registers. *The examiner asserts that in Levy's 3rd embodiment, when two threads are running, architectural registers are partitioned by thread such that while some may not be used, they are reserved for a specific thread. When only one thread is running, all of the physical registers are available for that thread.*

23. As per claim 9, Levy discloses the apparatus of claim 8 wherein the logical registers are allocated to the physical registers independently of the relative position of the logical registers to each other. *The examiner point to Fig. 15 as an example of Levy's invention allowing registers to be allocated independent of relative position.*

24. As per claim 10, Levy discloses the apparatus of claim 9 wherein the second means comprises a register allocation table (Fig. 4 table 72) to indicate the allocation of the logical registers to the physical registers. (Col. 9 lines 27-32)

25. As per claim 11, Levy discloses the apparatus of claim 9 wherein the second means comprises a plurality of register allocation tables (Fig. 15 tables 120 and 122) to indicate the allocation of the logical registers to the physical registers, each of the plurality of register allocation tables being associated with a separate thread of instructions.

26. As per claim 12, Levy discloses the apparatus of claim 11 wherein the first mode of operation is a single thread mode and the second mode is a multiple-thread mode.

27. As per claim 13, Levy discloses the apparatus of claim 12 wherein the first means is a register file comprising a list of the physical registers that are not allocated to the logical registers. (Fig. 4 free list 70 and Col. 9 line 31-32)

28. As per claim 14, Levy discloses the apparatus of claim 13 wherein the sum of the number of physical registers in the list and the number of logical registers associated with a single thread equals the number of physical registers within the physical register file. *The examiner asserts that when a single thread is running, Levy's 3rd embodiment ensures that all unused physical registers are accessible by said first thread. Therefore, the sum of the available threads (those in the free list) plus those in use by the first thread equal the total number of physical registers in the register file.*

29. As per claim 15, Levy discloses the apparatus of claim 14 wherein a first physical register is indicated in the list after an instruction associated with data stored in the first physical register is retired. (Col. 16 lines 39-44) *The examiner asserts that since a register's "contents may be overwritten" the register is added to freelist 70.*

30. As per claim 16, Levy discloses a system comprising: a memory unit to store a first and second thread of instructions (Fig. 1 instruction cache 24); a processor to perform the first and second thread of instructions (Fig. 1), the processor comprising a physical register file (Fig. 1 register file 37) wherein data corresponding to the first and second thread of instructions are stored in an order independent of whether the processor is in a multithread (MT) mode or a single-thread (ST) mode.

31. As per claim 17, Levy discloses the system of claim 16 wherein the processor further comprises at least one register allocation table (RAT) (Fig. 4 register mapping table 72) to indicate allocation of the data from logical registers to physical registers within the physical register file. (Col. 9 lines 27-32)

32. As per claim 18, Levy discloses the system of claim 16 further comprising a list of physical registers not allocated to a logical register (Fig. 4 free list 70), entries in the list being completely allocated to the first thread while the processor is in ST mode and entries in the list being partitioned such that a first portion of the entries are allocated to the first thread and a second portion of the entries are allocated to the second thread while the processor is in MT mode. *Levy's 2nd embodiment (described in Col. 10 lines 5-17 and pictured in Fig. 5B) fulfills the requirements of this claim. When only one thread is running, that thread has access to all of the renaming registers common to any running threads. When two threads are running, they share the common renaming*

registers and a partition can be made between registers associated with the first and second threads.

33. As per claim 19, Levy discloses the system of claim 18 wherein a first portion (Fig. 5B registers 86 in combination with the renaming registers) of all of the physical registers in the physical register file are allocated to the first thread and a second portion (Fig. 5B registers 88) of all of the physical registers in the physical register file are allocated to the second thread if the processor is in ST mode, the first portion of all of the physical registers being larger than the second portion of all of the physical registers. *The examiner asserts that if the processor is in ST mode, only one thread is running. This thread, therefor, has exclusive access to the shared renaming registers. Since the 2nd embodiment discloses that each thread has reserved architectural registers, regardless of whether there is an active thread associated with said thread or not, each of the first and second thread has a portion of the physical register file reserved for it.*

34. As per claim 20, Levy discloses the system of claim 19 wherein the second thread is dormant if the processor is in ST mode. *The examiner asserts that if the processor is in Single-thread mode, only one thread is running. Inherently, any second thread cannot be running, and must therefor be dormant.*

35. As per claim 21, Levy discloses the system of claim 19 wherein the first portion of all of the physical registers within the physical register file remain allocated to the first thread after the processor transitions to MT mode until instructions associated with data within the first portion of all of the physical registers within the physical register file are retired. *The examiner asserts that the processor disclosed by Levy inherently does not reallocate a currently used physical register to a newly started thread until the instruction(s) associated with said register are retired. (Col. 16 lines 39-44)*

36. As per claim 22, Levy discloses the system of claim 21 wherein the physical registers associated with the retired instructions are indicated within the list of physical registers. (Col. 16 lines 39-44) *The examiner asserts that since a register's "contents may be overwritten" the register is added to freelist 70.*

37. As per claim 23, Levy discloses a method comprising:

initializing a register allocation table (RAT) to map a first group of logical registers to a second group of physical registers; *Fig. 15 is evidence of such a mapping.*

dividing a freelist of registers in half if a processor associated with the free list is in multi-thread (MT) mode; *Levy's embodiment 1 discloses segregating rename register by thread.*

undividing the freelist of registers if the processor is in single-thread (ST) mode. *Levy's 2nd embodiment discloses an undivided rename register region. If*

the processor is in ST mode, the single thread has access to all of said rename registers.

38. As per claim 24, Levy discloses the method of claim 23 further comprising transitioning from ST mode to MT mode, the second group of physical registers being interspersed throughout a physical register file. *Figure 15 is an example disclosing physical registers spread throughout the register file with multiple threads running. The registers associated with the first thread are spread throughout the register file.*

39. As per claim 25, Levy discloses the method of claim 24 wherein the second group of physical registers remain interspersed throughout the physical register file after the transition from ST to MT mode. *The register file in Figure 15 exemplifies the physical registers being spread out throughout the file, regardless of what thread they are associated with.*

40. As per claim 26, Levy discloses the method of claim 23 further comprising transitioning from MT mode to ST mode, the second group of physical registers being interspersed throughout a physical register file. *The examiner asserts that in Figure 15, when the second thread terminates, the first thread's logical registers will still point to the same physical registers as "a register can only be freed when the hardware can guarantee that the register's value is 'dead'" (Col. 16 line 41-42)*

41. As per claim 27, Levy discloses the method of claim 26 wherein the second group of physical registers remain interspersed throughout the physical register file after the transition from MT to ST mode. *The examiner asserts that in Figure 15, when the second thread terminates, the first thread's logical registers will still point to the same physical registers as "a register can only be freed when the hardware can guarantee that the register's value is 'dead'" (Col. 16 line 41-42)*

42. As per claim 28, Levy discloses the method of 23 wherein the logical registers are allocated to the physical registers independently of the relative position of the logical registers to each other. *Figure 15 is evidence of physical registers being mapped to logical registers with no regard for physical location relative to each other.*

43. As per claim 29, Levy discloses the method of claim 28 wherein the sum of the entries in the freelist and the number of logical registers associated with a single thread equals the number of physical registers within the physical register file. *The examiner asserts that when a single thread is running, Levy's 3rd embodiment ensures that all unused physical registers are accessible by said first thread. Therefore, the sum of the available threads (those in the free list) plus those in use by the first thread equal the total number of physical registers in the register file.*

44. As per claim 30, Levy discloses the method of claim 29 further comprising a indicating a first physical register in the freelist after an instruction associated with data

stored in the first physical register is retired. (Col. 16 lines 39-44) *The examiner asserts that since a register's "contents may be overwritten" the register is added to freelist 70.*

Conclusion

45. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dillon Cody whose telephone number is 571-272-8401. The examiner can normally be reached on Mon - Fri, 8 AM - 5 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJC

RICHARD L. ELLIS
PRIMARY EXAMINER